Analog Design in a Digital Environment

Dennis Bohn
Paul Mathews
Rick Jeffs
Rane Corporation
Our Trio

• Dennis Bohn, CTO
  – Analog designer’s dilemma

• Paul Mathews, Sr. Analog Design Engineer
  – Faraday, Ampere and other old dead guys you “Ott” to know

• Rick Jeffs, Sr. Analog Design Engineer
  – Translating to schematics and layouts
Overview

• Two hour glimpse into a 20 week course
• Tutorial restricted to pro audio signal processing units in rack-mount format. (Other formats require different solutions.)
• Compare analog-only vs. mixed analog-digital designs.
• Review key audio parameters.
• Discuss magnetic & electric fields.
Overview

- Floor planning is critical to success.
- Passive solutions: shielding, filters, & layout solve the biggest problems.
- Protection tips against ESD
- Proven input and output stages.
- Selecting op amps that help rather than hurt.
Overview

• Nothing new here. Electric & magnetic field induced problems always existed but were usually negligible.
• Basic physic principals show how to reduce the magnitude of today’s problems to manageable levels.
• Layers of protection attenuate the problems
• Same solutions reduce radiated noise while improving immunity
References

• This PowerPoint Presentation available at www.rane.com/library.html
• Includes extensive references for further reading and study on EMI & ESD design.
  See “Analog Tutorial 2005 References”
• New AES page: www.aes.org/tutorials
• Several graphs used by permission from Keith Armstrong, Cherry Clough Consultants.
General References

• Williams, Tim, *EMC for Product Designers, 3rd Ed.* (Newnes, ISBN 0750649305)
Advanced References I

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That Was Then, This Is Now

• THEN
  – Opamps, VCAs, linear power supplies
  – 20Hz to 100kHz BW
  – Reducing hum, noise & the occasional click

• NOW
  – DSPs, microcontrollers, PLDs, switchmode power supplies
  – DC to daylight bandwidths
  – Reducing hum, noise, emissions, EMI susceptibility and protect against ESD
What Changed?

• Technology Changed
• Bureaucracy Changed
• Radiated & Conducted Emissions
• Radiated & Conducted Immunity
• Electrostatic Discharge (ESD) Protection
Digital Environment

- rectifiers and phase-angle power control
- microprocessor clocks and their harmonics
- switch-mode convertors and their harmonics
- Taxis, walkie-talkies
- mains harmonics and signalling
- actual signal spectrum
- audible spectrum
- 50Hz

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Op Amp in Analog Environment
Op Amp in Digital Environment

EMI in 1

EMI in 2

EMI in 4

EMI in 3

EMI in 5

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Analog-Only Product

Analog Signal Processing

\[ \begin{align*}
    f_{\text{max}} &< 100 \text{ kHz} \\
    \text{dv/dt max} &\sim 1.5 \text{ V/µs} \\
    \text{(20 kHz @ +20 dBu)}
\end{align*} \]

Linear Power Supply

\[ \begin{align*}
    \text{dv/dt} & = 340 \text{ V/5 ms} \\
    \text{di/dt} & = 1 \text{ A/5 ms}
\end{align*} \]

Simple & Cheap

±15 V

Front Panel Controls

Emissions

~None

Immunity

~Easy

Chassis

Simple & Cheap

Line Cord

?? DADT
Analog-Digital Product

Emissions
Many & Complex

Immunity
Difficult

Chassis
Complex & Expensive

Input

Output

A/D

D/A

Digital I/O

SMPS

dv/dt = 400 V/40 ns
= 10,000 V/µs
di/dt = 1 A/40 ns
= 25 A/µs
Complex & Expensive

+5V_D +5V_A +3.3V +1.8V ±15V

DSP

100 MHz typ.
1 ns rise times

Host µP

50 MHz typ.
1 ns rise times

Line Cord

56 µV max

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Every year it gets harder …

• Must use consumer ICs
• Every year they increase clock speeds, decrease size, operate from lower power supplies and discontinue last year’s parts.
• Leads to designing product as an integrated system that is bulletproofed against EMI & ESD, i.e., chassis & connectors must take brunt of EMI & ESD
And to make matters worse ...

• Increasing transistor density and speed, while decreasing power consumption for portable use, power supply voltages have dropped from +5V to +3.3V to +1.8V, increasing EMI susceptibility.

• Requiring less voltage and current to change states means less magnetic energy is required for false triggering.
**Rise Times are the Problem**

- It isn’t the clock frequency that hurts, it is the edges, i.e., the rise & fall times.
- Each year clock speeds may stay the same, but rise times decrease.
- A 1 kHz square wave with 1 ns rise & fall times generates damaging EMI.
- Step response contains frequencies out to daylight & create magnetic fields.
- Any rapid change creates radiated problems.

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Important Audio Parameters

- Slew Rate
- Noise
- Loop Gain
- Gain Bandwidth Product
  (aka Unity Gain Bandwidth)
Slew Rate

Max rate of change of an amplifier’s output:

\[ \text{dv/dt}\big|_{\text{max}} \equiv SR = 2\pi f_{\text{max}} V_{\text{peak}} \]

or

\[ f_{\text{max}} = \frac{SR}{2\pi V_{\text{peak}}} \]

\[ f_{\text{max}} = 24 \text{ kHz for } SR = 1.5 \text{ V/µs } \& \text{ } V_{\text{peak}} = 10 \text{ V} \]

• Want enough SR, but not too much.

• Often large SRs = marginal stability.
Thermal (Johnson) Noise

White noise generated by any passive resistive element.

Noise voltage

\[ e_n = \sqrt{4kTRB} \]

- \( T \) = temperature in degrees Kelvin
- \( R \) = resistor value in ohms
- \( B \) = noise bandwidth in Hz
- \( k \) = Boltzmann’s constant
# Noise Voltage Useful Values

Spot Noise $\equiv 1$ Hz BW & room temp (24°C)  
(as found on data sheets; usually @ 1 kHz)

Wideband Noise $\equiv 20$ kHz BW & room temp

<table>
<thead>
<tr>
<th>Resistance</th>
<th>Spot Noise</th>
<th>Wideband Noise</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Volts</td>
<td>EIN</td>
</tr>
<tr>
<td>150 $\Omega$</td>
<td>1.57 nV/$\sqrt{\text{Hz}}$</td>
<td>0.22 $\mu$V</td>
</tr>
<tr>
<td>1 k $\Omega$</td>
<td>4 nV/$\sqrt{\text{Hz}}$</td>
<td>0.57 $\mu$V</td>
</tr>
<tr>
<td>10 k $\Omega$</td>
<td>13 nV/$\sqrt{\text{Hz}}$</td>
<td>1.8 $\mu$V</td>
</tr>
</tbody>
</table>
Op Amp vs. Resistor Noise

• Noise from the feedback and input resistors add (in an RMS fashion) to the total op amp output noise
• Don’t need low noise ICs if using large resistors.
• Don’t pay for something you don’t need.
Low Noise Design

• Take all gain immediately and make that the lowest noise op amp -- do NOT distribute gain

• Use small resistors to minimize thermal (Johnson) noise.

• If using large resistors to minimize current drain, *they* become your main noise source – NOT the op amp.
Loop Gain & Op Amp Parameters

- Loop Gain = difference between open-loop and closed-loop gain
- Op Amp Specifications:
  - Non-inverting input impedance: $R_{in} \times \text{loop gain}$
  - Output impedance: $R_o / \text{loop gain}$
  - Harmonic Distortion: THD / loop gain
- As you run out of loop gain, your input impedance drops, while your output impedance and THD rise = trouble.
Bandwidth

• Require enough BW for good PSR, CMR & output virtual ground driving impedance.
• But, too much BW can cause noise problems
Gain-Bandwidth Product (Analog-Only Design)

- **Max Open loop Gain**
- **Loop Gain**
- **Closed-Loop Gain**

**Voltage Gain (dB)**
- >40 dB
- 6 dB/oct (20 dB/decade)

**Frequency (Hz)**
- 20 kHz
- 3 MHz

- Want ~60° Phase Margin
Gain-Bandwidth Product
(Analog-Digital Design)

- Max Open loop Gain
- Loop Gain
- Closed-Loop Gain

Voltage Gain (dB)
- >30 dB
- 6 dB/oct (20 dB/decade)

Frequency (Hz)
- 1 MHz
- 30 MHz

Want ~60° Phase Margin
Selecting Op Amps For Audio

• Yesterday: ~10; Today: ~100
• Specifications
  Noise, slew rate & GBW
• Configuration
  Single, dual, quad, etc.
• Package
  DIP, TSOT, MSOP, SOIC, TSSOP, etc.
• Price
• Availability
• Second-Source
Fields of Dreams

Paul Mathews
Rane Corporation
This Section

• Fast moving charges make waves
• Magnetic fields
• Electric fields
• Design rules that work
Fields and Radiated Energy

- In the good old days, currents, voltages mostly confined themselves to intentional paths like wires and components

- Rapid changes in current or voltage cause magnetic and electric fields, leading to:
  - Wave behavior, propagation delays, cross-talk
  - Noise coupling, signal integrity problems
  - Efficiency losses, etc.
Ampere and Faraday

• Ampere: Magnetic force $\propto$ current
• Faraday: Magnetic flux rate of change $\propto$ voltage
• Some Implications:
  1. Changing currents $\leftrightarrow$ changing flux $\leftrightarrow$ back emf $\rightarrow$ impedance, i.e., inductance
  2. Changing flux $\leftrightarrow$ emf $\leftrightarrow$ coupling, i.e., mutual inductance
Magnetic Fields

• Currents always have associated B-fields and v.v.

• B-fields impede current changes and store energy, lengthening transition times, causing ringing (inductive impedance)

• B-fields couple energy, often unintentionally, causing cross-talk and other phenomena (mutual inductance)

• Impedance and coupling rise linearly with frequency: 1000x more important at MHz compared to kHz.
Electric Fields

- Voltages *always* have associated E-fields and v.v.

- E-fields **impede** voltage changes and store energy, lengthening transition times *(Capacitance)*

- E-fields **couple** energy, often unintentionally, causing cross-talk and other noise phenomena *(Parasitic capacitance)*

- E-field coupling rises linearly with frequency: 1000x more important at MHz compared to kHz.
• Designers are used to thinking in terms of voltages, so currents and B-fields get neglected

• For DSPs and other high speed logic, voltages low, currents high (due to unavoidably low line Z)

• If you don’t control inductances, you end up with both E-field and B-field problems:
  Voltages develop across $Z_L$, resonances
B-fields and Loop Area

- Currents always flow in loops

- Collapse loops → less inductance, less cross-coupling
B-fields and Coupling

• Problem: adjacent loops couple

• REAL problem: broadband transformer
Cancellation of B-fields

- Alternation of loop direction can cancel B-fields at a distance.

- As usual, effect is bidirectional: this structure ‘picks up’ less EMI.
Some Loop Subtleties

- Not just wires and traces: total path, including components, parasitics
- Different loops in different states
- Bypass caps keep loops small
- Many loops are non-obvious
- Loops can ‘share’ paths
‘Grounds’ and Return Current

- Concepts of *image current* and *return current* must be understood:
  - E-field ↔ currents (moving charge) ↔ B-field
  - Therefore, image currents flow in adjacent conductors
  - Ideal return path completes circuit and provides lowest energy condition for fields → no unwanted image currents

- GOOD Return Paths: stripline, microstrip, image plane

- BAD Return Paths: anything irregular or distant to signal path
‘Grounds’ and Return Current

These symbols obscure what really happens:

\[\text{Diagram of symbols}\]
‘Ground’ Planes

- Low inductance path for return currents
- E-field shield
- Reference for single-ended signals: analog AND digital
- Patch Antenna (OOPS!)
- Lower inductance path for return currents, higher capacitance, better shield
- However: you still must do sensible floor-planning and layout
- Other ground pours must be thoroughly via-stitched
Loop Areas on Boards

- Signal and return traces on single layer:
  - B-field perpendicular to board,
  - $A =$ square area enclosed

- Signal and return on different layers:
  - B-field in plane of board
  - $A = d \times l$ (d = interlayer distance, l = trace length)
  - Includes trace over/under plane

- Signal on board, return through chassis:
  - Not recommended
Slots and Moats

• Signal current in trace
• Return current in plane, \( \leftarrow \) takes detour here and around slot
• Unintended loops
• It could be worse
• Or not as bad, if cancellation occurs
Where are the loops?
Loops on the Board

- Major Loop 1: FET ON
- Major Loop 2: FET OFF

Probably making things worse: one counter-clockwise, one clockwise, a nice push-pull loop antenna!

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Loops on the Board Rev 1

- Major Loop 1: FET ON
- Major Loop 2: FET OFF
Where are the loops, really?
What can be done here?

- Use smaller, lower parts, SMT
- Position parts for cancellation of fields
- Use shielded magnetics, progressive and crossed windings

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B-field Gotchas

• Reducing L
  – Wide traces (to reduce L) → capacitance → parasitic currents → EMI
  – Moving things together (to reduce L) → components get closer together → capacitance rises → parasitic currents → EMI

• Reducing $di/dt$
  – Series resistors, beads raise impedance, can interfere with matching, increase cross-coupling susceptibility
  – Slower logic transitions → delays and possible timing violations
  – Slower power switching transitions → reduced efficiency → higher heat dissipation
Back to E-fields

• You can’t have B without E and vice versa: E-fields move charge, moving charge means B-field

• In the far field, B and E are components of a radiated wave

• Parasitic currents always obey \( I = C \frac{dv}{dt} \)

• How to diminish parasitic currents?
  ✓ Reduce C
  ✓ Reduce \( \frac{dv}{dt} \)
Reducing Capacitance

\[ C \propto \frac{kA}{d} \]

- **Reduce conductor areas, A:**
  - Traces, planes: narrower, smaller
  - Components: choose smaller
  - Chassis, shields: plastic housings, smaller shields
  - The Earth, human body, building, etc.: live with ‘em

- **Increase distance between conductors, d**
  - Trace to trace, layer to layer
  - Component to component

- **Dielectric constant, k**
  - Air: \( k = 1 \), most insulators, \( 5 > k > 1 \), including encapsulants
  - Water: \( k \approx 50 \), so beware of moisture
Reducing $\frac{dv}{dt}$

Parasitic currents always obey $I = C \frac{dv}{dt}$

- Make $dv$ smaller
  - Reduce supply voltages
  - Use low voltage signaling
  - Shield near ‘victim’

- Make $dt$ bigger
  - Slower logic families
  - Slew rate controls
  - Series resistors, beads, shunt capacitance
  - Controlled rate power switching
Reducing dv/dt (cont’d)

- Reduce ringing power $P = f \times \frac{L_i^2}{2} = f \times \frac{C V^2}{2}$
  - Minimize parasitic inductances and capacitances
  - Design of magnetics, design of layout, placement

- Minimizing ringing effects
  - Terminators for transmission lines
  - Snubbers absorb energy, lower frequency of ring
  - Clamps limit voltages (but large currents can flow)
Block Parasitic Currents?

Parasitic currents *always* obey \( I = C \frac{dv}{dt} \)

- This is *Current Source* behavior:
  - You *can’t* reduce parasitic currents using resistors: return currents to source through low Z or matching Z
  - If you don’t provide a return path, free space (\( Z = 377 \)) will be the path, i.e., EMI
  - You *can’t* reduce parasitic currents using resistors: return currents to source through low Z or matching Z

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E-field Gotchas

• Reducing C
  – Skinny traces (to reduce C) → inductance → impedance → voltage differences → E-field
  – Moving things apart (to reduce C) → traces get longer → inductance rises → etc.

• Reducing $dv/dt$
  – Series resistors raise impedance, can interfere with matching, increase cross-coupling susceptibility
  – Slower logic transitions → delays and possible timing violations
  – Slower power switching transitions → reduced efficiency → higher heat dissipation
  – Improved bypassing → some chips slew faster → EMI
1. **Keep E-field IN**: Shield held at constant potential relative to **victim**. Parasitic currents flow into low-Z shield structure which **must** also have path back to culprit.

2. **Control B-field**:
   
   a) **Provide high \( \mu \) path for flux**
      
      - Different materials for different frequencies

   b) **Counteract field with opposing field**:
      
      - Eddy currents
      - Criss-crossing paths

   ✓ Steel heatsink < 100kHz
   ✓ Ferrites
   ✓ Flux bands
   ✓ Special winding methods
   ✓ Layout tricks
Where to Put Shields

• Shield around the culprit
  + Short path for parasitic currents reduces loop area, but
  – Capacitance to shield is higher, so larger currents flow

• Shield around the victim
  + Farther away from culprit, so lower capacitance $\rightarrow$ less current $\rightarrow$ lower $V_{\text{noise}}$
  – Parasitic currents must still be returned to the culprit source, possibly over a longer path

• Shield both culprit and victim
  ± Best performance, with advantages and disadvantages of both
Doing Without Shields

• Orientation and placement for minimum coupling
  – Orient low $dv/dt$ side of ‘hot’ components toward potential victims
  – Place sources and victims far apart
  – Perpendicular placements for both $B$ and $E$

• Connect conductive structures to reference potentials
  – Chassis, subpanels, frames, heatsinks, unused pins, extra wires in cables
  – DC connection
  – AC connection: may require safety capacitors
  – Dissipative connection (beads and Rs) may reduce ringing
Cancellation of E-fields

• Differential drive
  ✓ Very little far-field radiation $\leftrightarrow$ low losses
  ✓ Performance depends on exact balance, symmetry $\rightarrow$ watch those eye diagrams

• Driven shields
  ✓ Neutralize capacitance and shield wires inside
  ✓ Shield itself may still radiate
  ✓ Difficult above a few kHz

• EMI cancellation circuits
  ✓ Example: flyback anti-winding
Rules to Live By

A few simple rules will greatly improve your success ratio

- Product Layout ‘Floor’ Planning Rules
- Circuit Planning and Paper Design Rules
- Circuit Design and Board Layout Rules
Rule 1: Do Floor Planning Early

- A good floor plan trades off conflicting objectives:
  - Reduce unwanted inductance and capacitance by shortening connections.
  - Reduce unwanted coupling (inductive and capacitive) by moving sources and potential victims apart.
  - Plan for ESD paths away from circuits.
General Floor Plan

Input

A/D

D/A

DSP

Output

SMPS

Host

Line Cord

Chassis Gnd

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Rule 2: Shield for E-fields

- Shields provide a short path for inevitable parasitic currents, i.e., minimum loop area.
- Shield planes can work well for circuit traces and low profile components.
  - E-fields follow minimum energy path ‘inside’ board
  - Provide low impedance structure, meaning capacitive currents don’t change voltage much, so radiation is weak.
Rule 3 Plan for ESD

- Insulate where possible: 20kV
- Provide short paths to ground, just as for parasitic currents
- Keep inductance and mutual inductance low, i.e., loops small and far apart
- Insert series R, L and T (transformers)
Rule 4: Minimize $di/dt$ and $dv/dt$

- Use slowest logic families and lowest practical voltages; slew rate controls set to minimum speed.
- Incorporate series resistors in all high rate signal lines (reduces both $di/dt$ and $dv/dt$).
- Use slowest practical clock rates and minimum power transistor gate drive.
- Design for low power consumption, including turning circuits off when not in use.
Rule 5: Layout power & clock first

- Layer ‘stackup’ assignment first of all.
- Bypass scheme is critical: more on this later.
- High repetition rate logic signals take precedence over less frequently switched, e.g., clock vs. data.
- Signals with fanout have higher loading, cannot tolerate high series R, will have higher currents.
- Inductance between circuit regions can be a good thing.
Rule 6: Minimize Loop Areas

• Often, current issues trump voltage issues, even if traces get longer
• Including components…not just traces
• Use integrated logic wherever possible
• Use stripline, microstrip, and other loop area reduction methods
• Often, planes work best for return currents
  – Currents take minimum energy path, path of least inductance, return currents ‘image’ the trace
  – Low inductance and IR drop
  – Provide E-field shielding (more on this later)
• Avoid ‘moats’ or ‘slots’ in planes; never route across them.
Rule 7: Minimize capacitances for high dv/dt nodes

• Skinny traces can be a good thing
  – Don’t go too far with narrowing traces: inductance can resonate and raise dv/dt

• Move high dv/dt traces, structures away from potential ‘victims’

• Narrow side to narrow side orientation preferred
Actively Solving the Passive Puzzle
(or The Way In is the Way Out)

Rick Jeffs
Rane Corporation
High Performance Audio in a Digital Environment

• Achieving excellent audio performance in a digital environment is largely a **passive puzzle**.
  – Floor planning
  – Proper Integration of active and passive EMI / ESD protection
  – Trace Layout
  – Power distribution, bypass and power planes
What you’re up against

- 0.00001 0.0001 0.001 0.01 0.1 1 10 100 1,000 MHz
- -50 -40 -30 -20 -10 0 dB

- 50Hz rectifiers and phase-angle power control
- mains harmonics and signalling
- microprocessor clocks and their harmonics
- switch-mode convertors and their harmonics
- actual signal spectrum
- audible spectrum

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The Big Picture

Switchmode PS:
\[ dv/dt = 10,000 \text{ V/us} \]
\[ di/dt = 25 \text{ A/us} \]

Conducted Emissions:
CM + DM attenuated to microvolts/microamps

Sensitive Front-end:
Gain = -12 to +60 dB
CMRR = Min. 40 dB

Digital Clocking:
\[ dv/dt = 5,000 \text{ V/us} \]

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The Key to a Successful Design

• Good Floor Plan and Layout
  – Relative topology location
  – Trace loop area and geometry
  – Power planes and bypass

• Proper use of passive components
  – Capacitors
  – Bead inductors
  – Transient Voltage Suppressors (TVS)

• Careful selection of topologies and Op amps
What is covered

- Floor Plan and Power Planes
- Layout issues
- Distributed regulation and bypass
- Protecting Inputs and Outputs
- EMI effects on active circuits
- Input topologies
- Output topologies
Locating Topologies (Floor Plan)
Adding Power Planes

- A good floor plan allows logical power plane layout
Layout Issues

• Loop area was not a major concern in low speed analog design
• Trace geometry and part location were not critical
• Both have a major impact on performance in combined analog and digital designs
• Power and ground planes help reduce loop area
Loop Area (B-field)

- **Emissions:**
  - Larger loop, stronger radiated magnetic field

- **Immunity:**
  - Larger loop, more induced current from radiated magnetic field, reduced immunity.
Trace and Part Location (E-field)

- Avoid crosstalk from…
  - digital circuits
  - power supplies
  - unfiltered signal lines (input and output)
- Keep trace structures and components as small as possible
- Locate traces and parts away from emission sources
- Power and ground planes help reduce coupling
Power Distribution and Bypass

• Several voltages distributed to multiple power planes
• Must maintain…
  – Low source impedance
  – Low ripple
  – Small loop area
• Difficult to achieve without a minimum of four layers
Distributed Regulation

• Distributed regulation provides local regulation and bypass at each power plane

• Advantages of distributed regulation include:
  – Reduced number of routed supply traces
  – Lower impedance and ripple at power plane
  – Smaller current loop area
  – Reduced emissions and susceptibility to interference
Distributed Regulation and Bypassing

- Reduces loop area and ripple
- Maintains low impedance at point of load
Distributed Regulation and Bypassing

- Effective operating range of regulators and bypass:
  - Active regulator: Tens of kHz
  - Bulk bypass: Hundreds of kHz
  - IC bypass: Up to 500 MHz
  - Distributed power plane capacitance: Above 500 MHz
Bypass Capacitors

• **Purpose**
  – Reduce Ripple
  – Reduce Loop Area

• **Limiting Factors**
  – ESR
  – Inductance

• **Self resonance**
  – \[ \frac{1}{2\pi\sqrt{LC}} \]
  – Trace adds 10 nH per inch
Protecting Audio Input and Output Stages

- Need to achieve a minimum attenuation of 40 dB
  - (CMR) DC to 1 GHz and differential RF.
  - Active within the effective bandwidth of the Op-Amps
  - Passive above the effective bandwidth Op-Amps
- Limit voltages to a safe level
  - Passive reduction of static from thousands to tens of volts
  - Passive reduction from tens of volts to levels safe for active circuits
EMI Effect on Active Stages

• Diode junctions in active devices detect and demodulate RF signals.

• Demodulated signals result in:
  – Audio spectrum interference
  – Noise and offset problems.

• Detection can occur on:
  – input, power supplies and outputs

• Prevention requires attenuating RF to levels below forward voltage drop of diode junctions
EMI Effect on Active Stages

- Low bandwidth and slew rate do not prevent effective RF demodulation

Figure 1 Real-life demodulation in an LM324 opamp

Radiated RF field immunity test to EN 61000-4-3 with 1kHz modulated carrier

S/N specification

% THD+N

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Four Fundamental Stages of Line-level Input

- Passive EMI / ESD Filter and Shield Termination
  - Attenuate radiated RF (10 MHz to 1GHz)
  - Clamp ESD (+/- 4kV touch and +/- 8kV air)
- Passive Filter / Attenuator
  - Attenuate RF (150 kHz to 30 MHz)
  - Scale input for following stages
- Passive Voltage Clamp
  - Ensure safe voltages for active input buffer
- Differential Amplifier
  - Provide CMR and buffer input
Typical Line-level Input Stage

- Important to match elements carefully

![Diagram of a line-level input stage with components and their connections.]

- **Radiated EMI / ESD Filter**
- **Conducted Filter / Attenuator**
- **Voltage Clamp**
- **Balanced Buffer**

- **INPUT A**
- **J1 XLR FEM**
- **+5**
- **-5**

10 MHz up
100 kHz to 30 MHz
DC to 1 MHz

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Filter Interaction

- Why two passive EMI filters?
Capacitors

Variation of Impedance with Cap Value
Impedance vs. Frequency
0805 - C0G (NP0)
10 pF vs. 100 pF vs. 1000 pF

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Ferrite Beads

- Appear as lossy resistive element at higher frequencies
- Pay close attention to saturation current

**Impedance-Frequency (Typical)**

BLM15A Series

![Graph showing impedance vs. frequency for different models of Ferrite Beads.](image)
1st Stage EMI / ESD Filter

- Attenuate incoming and outgoing signals above 10 MHz
- Prevent against damaging, high voltage transients (8 kV)
- Low-z, shield connection to chassis
- Smallest loop area
- Lowest Z return to chassis
Line-level Input Stage
2nd Stage Filter and Attenuator

- Filter remaining EMI above BW of active circuits (150 kHz to 30 MHz)
- Scale differential audio signal
- Provide high common-mode input impedance
- Small loops
- Good symmetry
Input Voltage Clamp

- Input ESD measures reduce 8k volt transients to 25 to 50 volts (still too high)
- Voltage clamp limits voltage to safe levels for amplifier
- Signal diode provides fast, low capacitance clamp to supplies
- TVS devices from supply to ground prevent supply pumping
• Some applications require clamping below the supply rails
• Use TVS diodes from input to ground
• If low capacitance is required, use signal diodes to isolate TVS diodes
Differential Amplifier

- Buffer the input filter/attenuator
- Provide active CMR
- Provide low Z drive for ADC
- Provide bias for ADC
- Op amp selection
  - Low noise
  - Adequate bandwidth
  - Good supply noise rejection
Active Common-mode Rejection

• CMR provided by:
  – Differential amplifier
  – ADC
Special Mic Input Considerations

- First stage of ESD must allow 48 volts
- DC blocking cap value based on source impedance
- R27 and R28 should be as large as noise spec allows
Four Fundamental Functions of Line-level Output

- **Post DAC Filter**
  - Buffer DAC outputs
  - Reduce CM error and Out-of-Band noise
- **Differential Line Driver**
- **Voltage Clamp (+/- 4kV touch and +/- 8kV air)**
- **EMI Filter and Shield Termination**
  - Attenuate radiated RF (10 MHz to 1GHz)
  - Attenuate conducted RF (150 kHz to 30 MHz)
Post DAC Filter

- 2nd Order Filter
- Reduces out-of-band noise
- Reduces common-mode noise
- Buffers DAC output

**Graph:**
- dB vs. kHz plot
- Audible spectrum with possible ultrasonic and RF content

**Diagram:**
- Circuit diagram of the Post D/A Filter
- Components labeled R16, R17, R18, R19, R20, R21, C3, C9, C10, and AGND
- Voltage nodes labeled Va and Vb

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Balanced Line Driver

- Low output impedance
- Balanced impedance
- High current drive
- High bandwidth
- Adequate phase margin
Op Amp Considerations

Figure 25. Open Loop Gain Margin and Phase Margin versus Load Capacitance
Op Amp Considerations

Figure 18. Output Impedance versus Frequency

- $V_{CC} = +15 \text{ V}$
- $V_{EE} = -15 \text{ V}$
- $V_{O} = 0 \text{ V}$
- $T_{A} = 25^\circ \text{C}$
EMI / ESD Filter and Shield Termination

- Often neglected
- Same requirements as input ESD/EMI protection
- Same shield termination requirement
- Provides passive termination above bandwidth of Op amp
Output Filter Similar to Input Filter

- Active Filter
- 2nd Filter
- 1st Filter

- dB
- MHz

- actual signal spectrum
- audible spectrum
- 50Hz rectifiers and phase-angle power control
- mains harmonics and signalling

- microprocessor clocks and their harmonics
- switch-mode convertors and their harmonics

- Taxis, walkie-talkies
- cell-phones

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Achieving High Quality Audio in a Hostile Environment Requires...

- Good Floor Planning and circuit layout
  - Relative topology location
  - Trace loop area and geometry
  - Power planes and bypass
- Understanding passive components
  - Capacitors
  - Bead inductors
  - Transient Voltage Suppressors (TVS)
- Careful design of active circuits
- Properly integrating all elements
References Available at www.rane.com/library.html

“Analog Tutorial 2005 References”